What Is Claimed Is:

1. A method for forming a dual damascene line structure, comprising the steps of:

forming an inter-metal dielectric including a first region and a second region on a semiconductor substrate;

forming a first hard mask material layer on an entire surface of the inter-metal dielectric;

removing the first hard mask material layer on the first region;

forming a second hard mask material layer on an entire surface of the inter-metal dielectric;

forming a hard mask to remove a portion of the first hard mask material layer on the second region;

etching the inter-metal dielectric of the first region to a first thickness using the hard mask;

exposing the inter-metal dielectric of the second region; and

etching the exposed inter-metal dielectric to simultaneously form a via hole and a trench having the via hole.

2. The method according to claim 1, wherein the via hole is formed to have a positive slope by using an inner profile of the hard mask.

3. The method according to claim 2, wherein the hard mask has a gradual slope within an inner portion of the first region.

4. The method according to claim 1, wherein the step of removing the first hard mask material layer on the first region is performed using a photoresist pattern of a minimum thickness enabling only the first hard mask material layer to be etched while the step of removing a portion of the first hard mask material layer on the second region is performed using a photoresist pattern of a minimum thickness enabling only the second hard mask material layer to be etched.

5. A method for forming a dual damascene line structure, comprising the steps of:

sequentially forming a diffusion barrier film, an inter-metal dielectric including a first region and a second region, and a first hard mask material layer on a semiconductor substrate having a lower metallic line formed within an insulating layer;

selectively removing the first hard mask material layer on the first region using a photoresist pattern;

depositing a second hard mask material layer on an entire surface of the inter-metal dielectric;

removing the first hard mask material layer on the second region to form a hard mask having a double pattern;

etching the inter-metal dielectric of the first region to a first thickness using the hard mask;

removing the hard mask on the second region; and

etching the inter-metal dielectric to simultaneously form a via hole and a trench having the via hole.

6. The method according to claim 5, wherein the inter-metal dielectric is formed of a low inter-metal dielectric material.

7. The method according to claim 5, wherein the hard mask is formed of one of Ti, TiN, Ta, TaN, and W.

8. The method according to claim 5, wherein the hard mask is formed at a minimum thickness enabling the inter-metal dielectric to be etched.

9. The method according to claim 5, wherein the step of removing the first hard mask material layer on the first region is performed using a photoresist pattern at a minimum thickness enabling only the first hard mask material layer to be etched.

10. The method according to claim 5, wherein the step of etching the second hard mask material layer is performed using one of a plasma including an activated gas consisting mainly of Cl_2+BCl_3 and a plasma including an activated gas consisting mainly of SF_6.

11. The method according to claim 5, wherein the step of depositing the second hard mask material layer forms an inner sidewall within the first hard mask material layer on the first region in a curved spacer shaped surface.

12. The method according to claim 11, wherein a thickness of the deposited second hard mask material layer is the same as a thickness of the first hard mask material layer.

13. The method according to claim 5, wherein the step of removing the first hard mask material layer on the second region forms a photoresist pattern at a minimum thickness enabling only the deposited second hard mask material layer to be etched.

14. The method according to claim 5, wherein the first hard mask material layer on the second region is simultaneously removed when the second hard mask material layer on the first region is etched to expose the inter-metal dielectric.

15. The method according to claim 5, wherein the inter-metal dielectric is formed by using a plasma including a first activated $C_aF_b+C_xH_yF_z$ (wherein a, b, x, y, and z are integers) gas combined with a second gas including O_2, N_2, and Ar.

16. The method according to claim 5, wherein the via hole is formed to have a positive slope by using an inner profile of the hard mask.

17. The method according to claim 16, wherein the hard mask has a gradual slope within an inner portion of a first region.

18. The method according to claim 1, further comprising the step of removing the second hard mask material remaining after forming the via hole and the trench.

19. The method according to claim 1, further comprising the step of depositing a metallic material within the via hole and the trench to form a plug and an upper metal line.